In the Claims

1. (Original) A method for establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset, said method comprising the steps of:

calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value;

testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value.

2. (Original) A method of claim 1 wherein the received signal carries a high definition television (HDTV) signal transmitted as a modulated vestigial sideband (VSB) signal formatted as a one-dimensional data constellation of symbols representing digital image data.

3. (Original) A method as claimed in claim 1 wherein said desired symbol timing recovery range is plus or minus 1 kHz.

4. (Original) A method as claimed in claim 3 wherein said preselected number of offset values is nine.

5. (Original) A method as claimed in claim 4 wherein said nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz.

6. (Original) A method as claimed in claim 1 further comprising steps of repeating the testing step for each of a plurality of symbol timing recovery algorithms.

7. (Original) A method as claimed in claim 6 wherein said plurality of symbol timing recovery algorithms comprises the Mueller and Muller algorithm and the Gardner algorithm.

8. (Original) A processor for establishing timing synchronism between a transmitter symbol clock and a local receiver symbol clock in a receiver for receiving a signal comprising a sequence of symbols at a symbol frequency and subject to exhibiting symbol frequency offset comprising:

means for calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value;

means for testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value.

9. (Original) A processor as claimed in claim 8 wherein the received signal comprises a high definition television (HDTV) signal transmitted as a one-dimensional data constellation of symbols representing digital image data.

10. (Original) A processor as claimed in claim 8 wherein said desired symbol timing recovery range is plus or minus 1 KHz.

11. (Original) A processor as claimed in claim 10 wherein said preselected number of offset values is nine.

12. (Original) A processor as claimed in claim 11 wherein said nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz.

13. (Original) A processor as claimed in claim 12 further comprising:

means for using a plurality of symbol timing detection algorithms for said testing; and

means for switching between said algorithms as desired to maximize the possibility of STR lock.

14. (Original) A processor as claimed in claim 13 wherein the switching means comprises means for selecting one of the plurality of detection algorithms before testing each of said preselected offset values.

15. (Original) A processor as claimed in claim 13 wherein said plurality of timing detection algorithms comprise the Mueller and Muller algorithm and the Gardner algorithm.